REMARKS

Upon entry of this Response, claims 1, 2, 5, 6, 9, 10, 12-18, and 28-36 are pending in the present patent application. Claims 1, 2, 5, 6, 10, 12, 15, and 16 are amended. Claims 28-36 are newly added. Claims 19-27 are canceled without waiver, prejudice, or disclaimer. Applicants reserve the right to present these canceled claims, or variants thereof, in continuing applications. Reconsideration of the presently pending claims in view of the following remarks is respectfully requested.

I. Summary of Telephone Interview

Applicants wish to thank Examiner Malzahn for time spent with Applicants' representative, Thomas Hildebrandt, Reg. No. 59,303, during a telephone interview conducted on February 14, 2012, regarding the above-identified Office Action. During the interview, Applicants' proposed amendments were discussed. The Examiner agreed that Applicants' proposed amendments would probably be sufficient to overcome the rejections indicated by the Office Action. However, the Examiner noted that a further search of the prior art would be necessary.

II. Rejections of Claims 1, 2, 5, 6, 9, 10 and 12-27 under 35 U.S.C. § 102(b)

On page 2 of the Office Action, claims 1, 2, 5, 6, 9, 10 and 12-27 are rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by *Wu* (U.S. Patent 5,659,780). Anticipation under § 102 "requires the disclosure in a single prior art reference of each element of the claim under construction." W.L. Gore & Associates, Inc. v. Garlock, Inc., 220 U.S.P.Q. 303, 313 (Fed. Cir. 1983). Applicants have canceled claims 19-27 without

waiver, prejudice, or disclaimer, thereby rendering their rejection moot. Applicants respectfully request that the rejections of claims 1, 2, 5, 6, 9, 10, and 12-18 be withdrawn for at least the following reasons.

A. Claims 1, 2, 5, 6, and 9

Independent claim 1, as amended, recites:

> 1. A media processing filter engine operable to perform filtering operations on an input data stream comprising blocks of media data, the filter engine comprising:
> a first memory unit operable to store blocks of media data and to output a first block of media data to be processed;
> a second memory unit operable to store blocks of media data and to output a second block of media data to be processed;
> ***a first multiplexer coupled to the output of the first memory unit and to the output of the second memory unit and operable to output a selected one of the first block of media data and the second block of media data;***
> ***a combiner coupled to the output of the first memory unit and to the output of the second memory unit and operable to output a combined block of media data corresponding to a portion of the first block of media data and a portion of the second block of media data;***
> ***a second multiplexer coupled to the output of the first multiplexer and the output of the combiner and operable to output a selected one of the combined block of media data and the selected one of the first block of media data and the second block of media data***; and
> a single instruction, multiple data (SIMD) processor operable to receive blocks of media data from the second multiplexer and to perform filtering operations on blocks of media data from the first and second memory units concurrently.

(*Emphasis added*). Applicants respectfully submit that *Wu* fails to show or suggest at least the elements emphasized above in amended claim 1.

In rejecting claim 1, the Office Action (p. 2) alleges:

> Relative to claims 1, 10 and 19, Wu's Fig. 1 illustrates a media, which includes video, (note col. 1, lines 13-15 nd 35-38) a processing filter engine (note col. 2, lines 17 -20) including a first memory unit (multi-port

memory M and the topmost output port that feeds rs21) and a second memory unit (multi-port memory M and the middle output port that feeds rs11) and a single instruction multiple port, SIMD, processor (note col. 1, lines 54-56 and the abstract).

FIG. 1 of *Wu* is reproduced below:

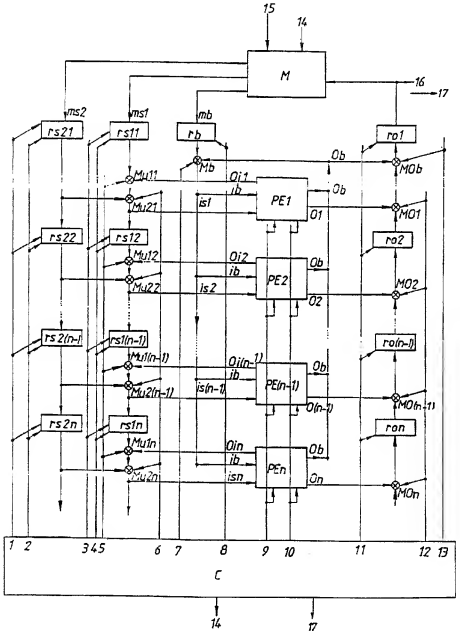

FIG. 1

Independent claim 1 has been amended to recite several additional elements, including a first multiplexer, a combiner, and a second multiplexer. This amendment is supported by FIG. 5 of the present application, along with its accompanying description. Although FIG. 1 of *Wu* appears to depict a multi-port memory M, *Wu* does not show or suggest that the multi-port memory M is operable in a split mode (where data from a first memory is separately accessible from data from a second memory) and a non-split mode (where data from the first memory and the second memory are combined). The first multiplexer of claim 1 enables the selection of data either from the first memory or from the second memory. The combiner of claim 1 combines a portion of the data from the first memory with a portion of the data from the second memory. The second multiplexer of claim 1 enables the selection of either the combined data from the combiner or the output of the first multiplexer. This hardware configuration does not appear to be shown or suggested by *Wu*.

Therefore, Applicants respectfully request that the rejection of claim 1 be withdrawn. In addition, Applicants respectfully request that the rejections of claims 2, 5, 6, and 9 be withdrawn as depending from allowable claim 1. Moreover, Applicants respectfully submit that dependent claims 2, 5, 6, and 9 recite further elements that patentably define over the prior art.

B. Claims 10 and 12-18

Independent claim 10, as amended, recites:

> 10. A media processing filter engine adapted to perform filtering operations on an input data stream comprising blocks of video data, the filter engine comprising:

a first memory unit operable to store blocks of video data and to output a first block of video data to be processed;

a second memory unit operable to store blocks of video data and to output a second block of video data to be processed;

a combiner coupled to the output of the first memory unit and to the output of the second memory unit and operable to output a combined block of video data corresponding to a portion of the first block of video data and a portion of the second block of video data;

a first shift register operable to receive and store a selected one of the first block of video data and the combined block of video data;

a second shift register operable to receive and store the second block of video data; and

a processor operable to receive blocks of video data from the first and second shift registers and to perform filtering operations on blocks of video data from the first and second shift registers concurrently.

(*Emphasis added*). Applicants respectfully submit that *Wu* fails to show or suggest at least the elements emphasized above in amended claim 10.

In rejecting claim 10, the Office Action (pp. 2-3) alleges:

> Relative to claims 10 and 19, the claimed first and second shift registers correspond to Wu's Fig. 1 shift registers rs21, rs22, ... rs2n and rs11, rs12, ... rs1n, respectively. Relative to the recited selective shifting by a predetermined number of bit corresponding to the number of bits used to represent one pixel note that when Wu's shift register rs21-rs2n receives the shift/load control signal 1 (col. 3, lines 37-38) the loaded data is shifted the number of bits that correspond to the pixel size.

Independent claim 10 has been amended to recite several additional elements, including a combiner, a first shift register, and a second shift register. This amendment is supported by FIGS. 5 and 6 of the present application, along with their accompanying description. Although FIG. 1 of *Wu* appears to depict a multi-port memory M, *Wu* does not show or suggest that the multi-port memory M is operable in a split mode (where data from a first memory is separately accessible from data from a second memory) and a non-split mode (where data from the first memory and the second memory are

combined). The combiner of claim 10 combines a portion of the data from the first memory with a portion of the data from the second memory. The first shift register receives either data from the first memory or combined data from the combiner. The second shift register receives data from the second memory. The processor receives data from the first and second shift registers. This hardware configuration does not appear to be shown or suggested by *Wu*.

Therefore, Applicants respectfully request that the rejection of claim 10 be withdrawn. In addition, Applicants respectfully request that the rejections of claims 12-18 be withdrawn as depending from allowable claim 10. Moreover, Applicants respectfully submit that dependent claims 12-18 recite further elements that patentably define over the prior art.

III. Newly Added Claims

Claims 28-36 are newly added through this Response. Applicants respectfully submit that claims 28-36 contain no new matter and are supported by the Specification. In addition, Applicants respectfully submit that claims 28-36 are allowable over the cited reference for at least the following reasons.

Independent claim 28 recites:

> 28. A system, comprising:
> a first data storage means configured to output a first block of data;
> a second data storage means configured to output a second block of data;
> ***means for outputting a selected one of the first block of data and the second block of data;***
> ***means for outputting a combined block of data corresponding to a portion of the first block of data and a portion of the second block of data;***

means for outputting a selected one of the combined block of data and the selected one of the first block of data and the second block of data; and

means for performing filtering operations on blocks of data from the first and second memory units concurrently.

(*Emphasis added*). Applicants respectfully submit that claim 28 is allowable for at least the reason that *Wu* fails to show or suggest at least the elements emphasized above. In addition, Applicants respectfully submit that claims 29-36 are allowable as depending from allowable claims 1, 10, or 28, respectively. Moreover, Applicants respectfully submit that dependent claims 29-36 recite further elements that patentably define over the prior art.

CONCLUSION

It is requested that all outstanding objections and rejections be withdrawn and that this application and all presently pending claims be allowed to issue. If the Examiner has any questions or comments regarding this Response, the Examiner is encouraged to telephone the undersigned counsel of Applicants.

Respectfully submitted,

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